Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microcomputer having an on-chip debugging function, comprising:

a central processing unit for executing instructions; and

a first monitor section which performs data transfer to and from a second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, said second monitor section being provided outside said microcomputer and performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

2. (Previously Presented) The microcomputer according to claim 1, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

3. (Previously Presented) The microcomputer according to claim 1, the first monitor section includes a control register used for execution of instructions in said central

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processing unit and having an address thereof allocated on a memory map in a debugging mode.

4. (Previously Presented) The microcomputer according to claim 2, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

5. (Previously Presented) The microcomputer according to claim 1, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

6. (Previously Presented) The microcomputer according to claim 2, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

7. (Previously Presented) The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

8. (Previously Presented) The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a

processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

9. (Previously Presented) The microcomputer according to claim 1, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

10. (Previously Presented) The microcomputer according to claim 2, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

11. (Previously Presented) The microcomputer according to claim 1, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

12. (Previously Presented) The microcomputer according to claim 2, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

13. (Previously Presented)The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

14. (Previously Presented) The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

15. (Cancelled).

16. (Previously Presented) The microcomputer according to claim 2, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

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17. (Previously Presented) The microcomputer according to claim 1, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. (Previously Presented) The microcomputer according to claim 2, said first monitor section includes a monitor RAM which is readable and writable, and when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 1;

an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said microcomputer.

20. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 2;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

21. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 3;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

22. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 5;

an input source of data to be processed by said microcomputer; and

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an output device for outputting data processed by said microcomputer.

23. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 7;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

24. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 9;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

25. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 11;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

26. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 13;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

27. (Currently Amended) An electronic instrument, comprising:

a microcomputer according to ~~claim 15~~claim 1;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

28. (Previously Presented) An electronic instrument, comprising:

a microcomputer according to claim 17;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

29. (Currently Amended) A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor section which performs data transfer to and from said second monitor section, determines a primitive command to be executed based on the receive data from said second monitor section, and performs processing for execution of the determined primitive command, wherein the second monitor section converts the debugging command into the primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section, said first monitor section includes a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization, and a circuit for sending and receiving data based on said first sampling clock, said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.

30. (Previously Presented) The debugging system according to claim 29, said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

31. (Previously Presented) The debugging system according to claim 29, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

32. (Previously Presented) The debugging system according to claim 29, the first monitor section includes a monitor RAM into which contents of an internal register of said

central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

33. (Previously Presented) The debugging system according to claim 29, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

34. (Previously Presented) The debugging system according to claim 29, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

35. (Previously Presented) The debugging system according to claim 29, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

36. (Previously Presented) The debugging system according to claim 29, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

37. (Previously Presented) The debugging system according to claim 29, said first monitor section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.